REMARKS

Claims remaining in the present application are Claims 1-12. No Claims have been amended or canceled. No new matter has been added as a result of these amendments.

CLAIM REJECTIONS

35 U.S.C. §102

In paragraph 4, Claims 4-6 and 10-12 are rejected under 35 U.S.C. §102(b) as being anticipated by USPN 4,247,926 by Gappa et al. (referred to hereinafter as "Gappa"). The rejection is respectfully traversed. It is respectfully submitted that Claims 4-6 and 10-12 are neither taught nor suggested by Gappa.

Independent Claim 4 recites:
A semiconductor device having a P-gate/P-substrate capacitor for characterizing polysilicon gate depletion corresponding to the semiconductor device, comprising:
a P doped substrate;
a gate oxide layer disposed over the P doped substrate;
a first isolation oxide and a second isolation oxide disposed over the P doped substrate;
a P+ doped gate disposed over at least one portion of the first isolation oxide, the gate oxide, and the second isolation oxide.

The cited reference fails to teach or suggest the claimed limitations as discussed below.

For example, at col. 3, lines 38-60, Gappa states:
... the first embodiment as shown in FIG. 1 is built in a single semi conductor substrate, P type semiconductor regions (referred to as P type well or wells, hereinafter) 2, 3 are formed in the major surface of an N type silicon unicrystal substrate 1 ... Turning now to the other P type well 3, an insulating film 10 of 100 A thick and made of an insulating material such as a silicon oxide is formed on the surface thereof. At the same time, a conductive layer 11 made of a metal such as aluminum or a polysilicon is formed on the insulating layer 10, so as to form a capacitor CO.

Further, FIGS. 2, 9, 10, 11, 13 and 14 of Gappa all show semiconductors with an N doped substrate 1, a P type well 3, insulating film 10 made of insulating material such as silicon oxide, and a conductive layer 11 made of a metal such as aluminum or a polysilicon that is formed on the insulating layer 10.

The Office Action states, "Figure 11 illustrates a semi conductor device having a p-gate (11) disposed over a first and second isolation oxide (28) a gate oxide (10). This structure is over a p doped substrate (3)." However, as already discussed element 11 is a conductive layer not a p-gate, element 10 is an insulating film not a gate oxide, and element 3 is a P type well of the N doped substrate 1 rather than a p doped substrate.

Thus, Gappa does not teach or suggest "a P doped substrate," "a gate oxide layer disposed over the P doped substrate," "a first isolation oxide and a second isolation oxide disposed over the P doped substrate," nor "a P+ doped gate disposed over at least one portion of the first isolation oxide, the gate oxide, and the second isolation oxide," as Claim 4 recites.

For the foregoing rationale, the limitations of Claim 4 are neither taught nor suggested by Gappa. As such, allowance of Claim 4 is respectfully solicited.

Claims 5 and 6 depend on Claim 4, which is believed to be allowable for the foregoing rationale. As such, it is respectfully asserted that the rejections of Claims 5 and 6 have been overcome and their allowance is earnestly solicited.

Independent Claim 10 recites:
A semiconductor capacitor structure, comprising:
an P doped substrate;
a gate oxide layer disposed over the substrate;
a first isolation oxide and a second isolation oxide disposed over the substrate;
a P+ doped gate disposed over the first isolation oxide, the gate oxide, and the second isolation oxide, wherein the semiconductor capacitor structure is used to characterize polysilicon gate depletion corresponding to a semiconductor process.

The cited reference fails to teach or suggest the claimed limitations of Claim 10 for similar reasons that the cited reference fails to teach or suggest the claimed limitations of Claim 4. As such, allowance of Claim 10 is respectfully solicited.

Claims 11 and 12 depend on Claim 10, which is believed to be allowable for the foregoing rationale. As such, it is respectfully asserted that the rejections of Claims 11 and 12 have been overcome and their allowance is earnestly solicited.

CLAIM REJECTIONS

35 U.S.C. §102

In paragraph 6, Claims 1-3 and 7-9 are rejected under 35 U.S.C. §102(b) as being anticipated by Gappa. The rejection is respectfully traversed. It is respectfully submitted that Claims 1-3 and 7-9 are neither taught nor suggested by Gappa.

Independent Claim 1 recites:
A semiconductor device having a N-gate/N-substrate capacitor for characterizing polysilicon gate depletion corresponding to the semiconductor device, comprising:
an N doped substrate;
a gate oxide layer disposed over the N doped substrate;;
a first isolation oxide and a second isolation oxide disposed over the N doped substrate and on opposing edges of the gate oxide layer;
an N+ doped gate disposed over at least one portion of the first isolation oxide, the gate oxide, and the second isolation oxide.

The cited reference fails to teach or suggest the claimed limitations as discussed below.

It is not clear what in Gappa corresponds to "a gate oxide layer disposed over the N doped substrate," a first isolation oxide and a second isolation oxide disposed over the N doped substrate," or "an N+doped gate disposed over ... the first isolation oxide, the gate oxide, and the second isolation oxide." For example, the Office Action states in paragraph 7, "Figure 11 illustrates a semiconductor device having a p-gate (11) disposed over a first and second isolation oxide (28) a gate oxide (10). This structure is over a p doped substrate (3)." However, paragraph 7 quotes features recited in Claims 4 and 10 rather than features recited in Claim 1. For the purposes of argument, Applicant shall compare element 3 of figure 11 to the "N doped substrate" in Claim 1, element 10 of figure 11 to "a first iisolation oxide and a second isolation oxide" in Claim 1 and element 11 of figure 11 to the "N+ doped gate" in Claim 1.

However, element 11 is a conductive layer not a p-gate, element 10 is an insulating film not a gate oxide, and element 3 is a P type well of the N doped substrate 1 rather than a N doped substrate.

For example, at col. 3, lines 38-60, Gappa states:
... the first embodiment as shown in FIG. 1 is built in a single semi conductor substrate, P type semiconductor regions (referred to as P type well or wells, hereinafter) 2, 3 are formed in the major surface of an N type silicon unicrystal substrate 1 ... Turning now to the other P type well 3, an insulating film 10 of 100 A thick and made of an insulating material such as a silicon oxide is formed on the surface thereof. At the same time, a conductive layer 11 made of a metal such as aluminum or a polysilicon is formed on the insulating layaer 10, so as to form a capacitor CO.

Further, FIGS. 2, 9, 10, 11, 13 and 14 of Gappa all show semiconductors with an N doped substrate 1, a P type well 3, insulating film 10 made of insulating material such as silicon oxide, and a conductive layer 11 made of a metal such as aluminum or a polysilicon that is formed on the insulating layer 10.

For the foregoing rationale, the limitations of Claim 1 are neither taught nor suggested by Gappa. As such, allowance of Claim 1 is respectfully solicited.

Claims 2 and 3 depend on Claim 1, which is believed to be allowable for the foregoing rationale. As such, it is respectfully asserted that the rejections of Claims 2 and 3 have been overcome and their allowance is earnestly solicited.

The cited reference fails to teach or suggest the claimed limitations of Claim 7 for similar reasons that the cited reference fails to teach or suggest the claimed limitations of Claim 1. As such, allowance of Claim 7 is respectfully solicited.

Claims 8 and 9 depend on Claim 7, which is believed to be allowable for the foregoing rationale. As such, it is respectfully asserted that the rejections of Claims 8 and 9 have been overcome and their allowance is earnestly solicited.

CONCLUSION

In light of the above listed amendments and remarks, reconsideration of the rejected Claims is requested. Based on the amendments and arguments presented above, it is respectfully submitted that Claims 1-29 overcome the rejections of record. Therefore, allowance of Claims 1-29 is earnestly solicited.

Should the Examiner have a question regarding the instant response, the Applicant invites the Examiner to contact the Applicant's undersigned representative at the below listed telephone number.

Respectfully submitted,
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